**CPU, Memory, and I/O Devices**

**All about the Computer**

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INTRODUCTION

Many professionals, in today’s society, use their computers as a major instrument that is relied on, daily, to, accomplish tasks, communicate with, colleagues, affiliates, and other stakeholders, and be entertained. Some of the greatest concerns, apart from security, is the ability to make the machine operate or behave in a way that is more fluid and less time consuming to perform a task.

This discussion answers the questions of, how can I browse the internet more quickly when using multiple tabs on a given web browser’s window, how can I make my programs run faster on my work computer, and how can I reboot the machine faster? These questions are answered with the exploration and understanding of the various inner workings of a computer and how they relate to various functions that the user is trying to accomplish.

THE CPU

The primary function of the CPU (Central Processing Unit) is to execute programs which are stored on the main memory. The CPU reads data, or instruction codes, from the main memory and decodes those instructions. The registers or the memory contain the necessary data to execute theses instructions.

Additionally, the CPU is responsible for controlling peripheral devices or I/O (Input/Output) devices. If the computer is small enough, the CPU can be comprised of a single microprocessor. Larger computers utilize multiple microprocessors, in parallel. In this way, computers are more powerful and faster.

For Sections of the CPU see, Figure 1.

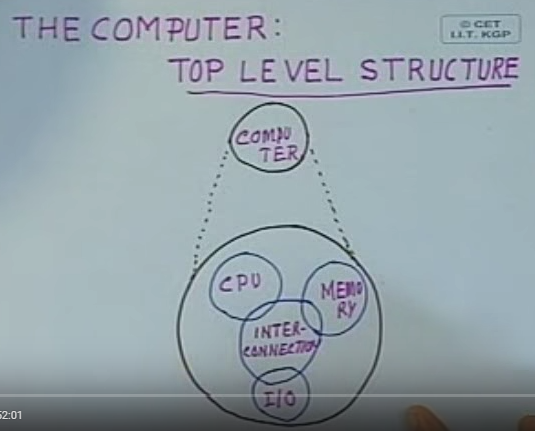


Figure 1: Parts of the CPU (Kashyap, 2012)

REGISTERS

Nothing more than a bunch of flip flops that store data.

1. General Purpose Registers
2. General Purpose – these have not been explicitly used. Can be used to store ***data***, ***address***.
3. Number of General Purpose registers
4. Number of bits – depends of size of processor (8 bit) register pair(can store 16 bit address)
5. Execution time will be decided by the number of General Purpose registers
6. Size – how many programs to be executed depends on the number of General Purpose registers.
7. Ease of program
8. Special Purpose Registers – used for a specific purpose (User Accessible)
9. Accumulator – used to store one of the operands
10. Program Counter – keeps track of the memory location
11. Status Register – will reflect the outcome of an instruction execution (data overflow, results positive or negative, etc)
12. Stack Pointer – used to implement the data structure (Stack – subroutine calls)

Another way to classify registers is, User Accessible or not.

(Not User Accessible)

1. Memory Address Register (**MAR**)
2. Memory Data Register (**MDR**)
3. Instruction Register (**IR**)
4. Temporary Register (**TR**)

Table 1: REGISTERS

|  |  |
| --- | --- |
|  | ACC (8 bit) |
| B (8 bit) | C (8 bit) |
| D (8 bit) | E (8 bit) |
| H (8 bit) | L (8 bit) |
| Program Counter (PC) (16 bit) | |
| Stack Pointer (SP) (16 bit) | |
|  | S - Z – AC – P – CY  CY 🡪 Carry  P 🡪 Parity  AC 🡪 Auxiliary Carry  Z 🡪 Zed or Zero  S 🡪 Sign (+/-) |

ARITHMETIC AND LOGIC UNIT

ARITMETIC OPERATIONS

1. Addition
2. Subtraction
3. Increment
4. Decrement

TIMING AND CONTROL UNIT

LOGICAL OPERATIONS

1. AND
2. OR
3. XOR
4. NOT
5. CLEAR
6. COMPARE
7. SHIFT
8. ROTATE

PROGRAM COUNTER

The Program Counter (PC) is a *special purpose register*. This register contains the address location, in memory, of the next instruction to be executed by the CPU. Assuming normal execution of the current instruction, the CPU fetches the opcode form the Read-only memory (ROM), the PC’s content is automatically incremented, sequentially (ROM, 2007).

Figure 2 is an illustration of a program counter.

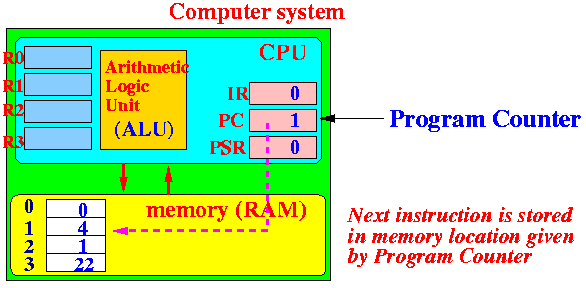


Figure 2: Program Counter

The PC is 16 bits wide meaning that it can access program addresses 0000 to FFFFH – a total of 64k bytes of code (8051 architecture, 2012).

STACK POINTER

A stack pointer is a small register that’s job is to hold or store the address of the last program request in a data structure called a stack (Gibilisco, 2012). The stack is a data structure that stores data from the top down. The data is pushed onto the stack and popped off. This provides the concept of last-in first-out or LIFO.

STATUS/FLAG REGISTER

The Status Register or Flag Register of the CPU is a hardware register and it is abbreviated as P. The resulting condition of any of the three results from the, arithmetic, logical, or command operations, from the ALU, is the condition of the CPU. These, most current, conditions are recorded within the Flag Register. The Flag Register is also responsible for the enabling and disabling of interrupts and setting the CPU operating mode (Sander, n.d.).

SEMICONDUCTOR MEMORY

During the years, 1955 – 1975, magnetic-core memory was the most widely accepted and used form of random-access memory (RAM) (ROM, 2007).

See illustration in Figure 3.

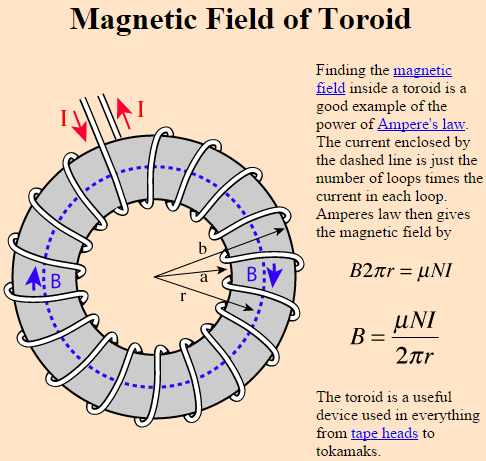


Figure 3: Magnetic Core (<http://hyperphysics.phystr.gsu.edu/hbase/magnetic/toroid.html>)

These tiny magnets, toroids or rings, which are the cores, represent bit values of either 1 or 0. They are either charged positively or negatively, as current passes through them, and their bit value is associated as 1 or 0 respectively.

This type of memory was commonly known as core memory, or simply, core. The process of reading from the core caused all of the toroids to be reset to 0; thus, erasing the memory. This was known as destructive readout. Since the creation, production of Integrated Circuits (ICs), core memory has been superseded by various types of RAM.

Static RAM is a type of fast access memory that requires a constant power source. The data is stored in a series of transistors that remember the signal given to them with a standard power signal. This type of RAM has a higher cost, but a significantly higher speed and its typically employed in the L2 cache. This cache is relatively small, keeps costs down, and lives in the CPU (Lewis, 2010).

Dynamic RAM is the most common form of RAM used in computing technology like Desktop PCs and Laptops. Unlike Static RAM, it’s a little slower, needs to be refreshed, and utilizes capacitors that hold data for a finite amount of time (about 15 nanoseconds). Memory is maintained with the reapplication of electricity/power. The slight loss of speed is made up for in its reduced costs.

Single data rate synchronous dynamic random-access memory (SDR SDRAM) transfers data through the control of the timing of the electrical signals and the clock signals. Through innovation and refinement, higher transfer rates have been achieved by a more strict control of the timing of electrical data and clock signals; for example, implementations of phase-locked loops and self-calibration allows for double pumping to lower clock frequencies. Double pumping is the term given to transferring data on the rising and falling edges of the clock signal.

The most used type of Dynamic RAM is DDR4 SDRAM, the successor to double data rate synchronous dynamic random-access memory (DDR SDRAM). DDR1, DDR2, DDR3, and DDR4 have chronologically double their speeds, but are not forward or backward compatible.

Up until April 20, 2015, the DDR SDRAM series had been the fastest available memory on the market. Now, with the application of resistors there is a new type of memory that suggests users will be able to store up to about 100 times more data on their smart phones (Gibb, 2015).

This new technology is called, Resistive RAM or ReRAM. It is operates with low power consumption and takes up a very small amount of physical space. Its initial release is set into the niche environment of portable health care applications, security equipment, and sensor equipment. This type of release will not have an immediate impact on DDR RAM in the current market place; at least, not in the near future (Gibb, 2015).

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